GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER– III(NEW) EXAMINATION – WINTER 2022

Subject Code:3130306   **Date:27-02-2023**
Subject Name:Fundamentals of Digital Electronics
Time:02:30 PM TO 05:00 PM   **Total Marks:70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Subtract the following Binary numbers using 1's complement method, 111000101-101101	**03**
	(b)	Explain Universal Gates with truth table.	**04**
	(c)	Explain Full Adder with truth table and Logic Diagram.	**07**
Q.2	**(a)**	Encode data bits 1010 into the 7-bit even parity Hamming code.	**03**
	(b)	Prove De Morgan theorem with truth table.	**04**
	(c)	Explain Full Subtractor with truth table and Logic Diagram.	**07**
		OR	
	(c)	Design 3-bit Magnitude Comparator.	**07**
Q.3	**(a)**	Draw logic diagram of Boolean expression $f = A + A\overline{BD} + \overline{ABC} + AB\overline{CD}$.	**03**
	(b)	Expand f = C (A+B) to maxterms and minterms.	**04**
	(c)	Design 16:1 MUX using 4:1 MUX (Multiplexer) Modules.	**07**
		OR	
Q.3	**(a)**	Explain Octal to Binary Encoder.	**03**
	(b)	Explain 3-Line to 8-Line Decoder with logic Diagram.	**04**
	(c)	Find the minimal expression for $f = \sum m\{2,3,4,7,11,12,13\}$ using Kmap.	**07**
Q.4	**(a)**	Explain D Flip –flop.	**03**
	(b)	Reduce the Boolean Expression $f = \sum m\{0, 2,3,4,7\}$ using tabular Method.	**04**
	(c)	Design 4-bit Gray to Binary Code Converter.	**07**
		OR	
Q.4	**(a)**	Implement Half adder with Programmable Logic Array.	**03**
	(b)	Explain Serial IN, Serial Out shift register.	**04**
	(c)	Explain Positive Edge triggered S-R and J-K Flip Flops.	**07**
Q.5	**(a)**	Write Excitation Tables of J-K Flip Flop and T-Flip Flop.	**03**
	(b)	Explain Master- Slave J-K flip flop.	**04**
	(c)	Design Asynchronous Two-bit Ripple UP-Counter using Negative Edge-triggered J-K Flip-Flops.	**07**
		OR	
Q.5	**(a)**	Explain Applications of Flip Flops.	**03**
	(b)	Describe Conversion of J-K flip flop to T flip flop.	**04**
	(c)	Design Synchronous 3-bit UP Counter using JK flip flop.	**07**

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