Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III(NEW) EXAMINATION – WINTER 2022

Subject Code:3131102 Date:24-02-2023

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	State and prove De-Morgan's Theorem.	**03**
	(b)	Differentiate between combinational and sequential circuits.	**04**
	(c)	Simplify the following Boolean expression by means of the Tabulation method. $F(A,B,C,D) = \sum m(1,2,5,6,7,8,9,11,12,13,15)$	**07**
Q.2	**(a)**	Convert as below I. $(110101010)_2 = (\ )_8 = (\ )_{16}$ II. $(673.10)_8 = (\ )_2$ III. $(ABF)_{16} = (\ )_{10}$	**03**
	(b)	Show that NAND & NOR are universal gates	**04**
	(c)	Minimize the following function in SOP minimal form using K-Maps: $F(A, B, C, D) = \sum m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)$	**07**
		OR	
	(c)	Design a 4 bit binary to gray code converter and implement using EX-OR gates only.	**07**
Q.3	**(a)**	Give comparison of TTL and CMOS family.	**03**
	(b)	Explain half adder & half subtractor circuit.	**04**
	(c)	Explain about JK & RS Flip Flop circuit using its symbol, block diagram, truth table and characteristics equation.	**07**
		OR	
Q.3	**(a)**	Derive excitation tables for R-S, J-K and T flip-flops.	**03**
	(b)	Compare ROM, PLA and PAL.	**04**
	(c)	Design a counter to generate the repetitive sequence 0,1,2,4,3,6.	**07**
Q.4	**(a)**	Discuss general state machine architecture	**03**
	(b)	Implement the 8× 1 MUX using two 4 ×1 MUX.	**04**
	(c)	Describe working principle of Programmable Logic Array with block diagrams.	**07**
		OR	
Q.4	**(a)**	Define: Register, Ripple counter, Synchronous counter.	**03**
	(b)	Implement Full Adder using 3×8 decoder.	**04**
	(c)	Explain the types Finite machines.	**07**

Q.5	**(a)**	Compare asynchronous and synchronous state machines.	**03**
	(b)	Implement T flip flop using D flip flop.	**04**
	(c)	Describe the operation of 4-bit bidirectional shift register with logic diagram.	**07**

OR

Q.5	**(a)**	Define: i) Fan-in ii) Fan-out iii) Propagation delay	**03**
	(b)	Explain working of Toggle flip-flop with characteristic table and logic diagram.	**04**
	(c)	Explain dual slope type A/D converter in detail.	**07**

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