

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER- III(NEW) EXAMINATION – WINTER 2022

Subject Code:3130704

Date:27-02-2023

Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM

Total Marks:70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

	Marks
Q.1 (a) Implement NOR, AND, & OR gates using NAND gates only	03
(b) Write the boolean expression for the logic diagram given below and simplify it as much as possible and draw the logical diagram that implements the simplified expression	04
(c) Do as directed:	07
1. Convert $(75.75)_{10} = (___)_8 = (___)_{16}$	
2. Convert $(101.10)_{16} = (___)_8$	
3. Add $(17)_{10}$ and $(-25)_{10}$ using 8-bit 2's complement	
Q.2 (a) Explain SR flip-flop using characteristic table & characteristic equation	03
(b) Explain 4-bit parallel binary adder with neat and clean diagram	04
(c) Obtain the set of prime implicants for Function $F = \sum m(1,2,3,5,6,7,8,9,12,13,15)$	07
OR	
(c) A combinational logic circuit is defined by the functions: $F1 = \sum (0,1,2,4)$ and $F2 = \sum (0, 5, 6,7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs.	07
Q.3 (a) Differentiate synchronous counter and asynchronous counter	03
(b) Explain BCD adder using two 4-bit adder IC and a correction -detector circuit	04
(c) Do the conversion of JK flip flop to T flip flop and D flip flop to JK	07
OR	
Q.3 (a) Design 4 X 16 decoder using two 3 X 8 decoders	03
(b) List and explain in detail Binary codes with example	04
(c) Design mod-6 asynchronous counter using T flip flop	07
Q.4 (a) Reduce the expression $\sum (2, 3, 6,7,8,10,11,14)$ using K-map	03

- (b) Do as directed: **04**
 1. Add 25+17 in BCD
 2. Add 37 +28 in XS-3
- (c) With a neat block diagram explain the function of encoder. Explain priority encoder? **07**

OR

- Q.4** (a) Explain R-2R ladder type D/A converter **03**
 (b) Implement the following Boolean functions with a 3 x 1 multiplexer F (w, x, y, z) = $\Sigma (2, 3, 5, 6, 11, 14, 15)$ **04**
 (c) Design Combinational circuit for Binary to XS-3 conversion **07**

- Q.5** (a) Compare TTL, ECL, & CMOS logic families. **03**
 (b) Draw truth table of 2-bit digital comparator **04**
 (c) List out various commonly used D/A converters. Draw & explain any one D/A converter. **07**

OR

- Q.5** (a) A combinational logic circuit is defined by the functions: **03**
 $F1 = \Sigma (0,1,2,5,7)$ and $F2 = \Sigma (1, 2,4, 6)$. Implement the circuit with a PROM
 (b) Explain types of shift-register and their application **04**
 (c) List out various commonly used A/D converters. Draw & explain any one A/D converter **07**