Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III(NEW) EXAMINATION – WINTER 2022

Subject Code:3130907 Date:24-02-2023

Subject Name:Analog & Digital Electronics

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Define the following a)Input Offset Current b) Slew Rate c)Input Bias Current	**03**
	(b)	Explain the ideal voltage transfer characteristics of Op-Amp.	**04**
	(c)	Draw the block schematic of a typical operational amplifier Op-Amp and briefly explain the function of each block.	**07**
Q.2	**(a)**	Explain the procedure of offset voltage compensation in an op amp.	**03**
	(b)	Explain voltage follower with it's application.	**04**
	(c)	Draw and explain working of Op-amp base Wien Bridge oscillator with it's advantages and application.	**07**
		OR	
	(c)	With neat circuit diagram explain the working of an Integrator with relevant waveforms.	**07**
Q.3	**(a)**	Implement the following logic function using the 8:1 multiplexer. $F(A,B,C) = \Pi M(0,1,3,5,7)$	**03**
	(b)	Minimize the following expression and realize using basic gates. $Y=\Sigma\ m(0,2,5,6,7,8,10,13,15)$	**04**
	(c)	Simplify the Boolean function $F= \overline{A}\overline{B}\overline{C} + A\overline{B}D + \overline{A}\overline{B}C\overline{D}$ using don't care conditions $d= ABC + A\ \overline{B}\overline{D}$ in 1) Sum of products (SOP)and 2) Product of sums(POS) by means of K Map and implement it with no more than two NOR gates. Assume that both the normal and complement inputs are available.	**07**
		OR	
Q.3	**(a)**	Compare Multiplexer and Demultiplexer.	**03**
	(b)	Explain how Demultiplexer can be used as a 3:8 Decoder.	**04**
	(c)	Derive full subtractor with the help of necessary truth table and K –map. Also express in terms of logic diagram.	**07**
Q.4	**(a)**	What are Preset and Clear inputs with flip flop? Why are they provided with flip flop?	**03**
	(b)	Classify the various modes of operation of shift register.	**04**
	(c)	Explain the working of Master Slave JK flip flop.	**07**
		OR	
Q.4	**(a)**	Differentiate between combinational logic circuit and sequential logic circuit.	**03**

	(b)	Write a short notes on Parallel in serial out shift register.	**04**
	(c)	Explain S R flip flop with it's working operation.	**07**
Q.5	**(a)**	Compare various D/A converters.	**03**
	(b)	Define 3- bit parity generator circuit using even parity bit.	**04**
	(c)	Explain R-2R ladder DAC with necessary diagram.	**07**
		OR	
Q.5	**(a)**	Define following specification of ADC 1)Conversion Time 2)Resolution 3)Quantization	**03**
	(b)	State the difference between Asynchronous and Synchronous counters.	**04**
	(c)	Explain working of Successive approximation type ADC	**07**

.