Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2021

Subject Code:3130306 Date:23-02-2022

Subject Name:Fundamentals of Digital Electronics

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Perform the following: (i) Convert the decimal number 68.16 into binary number. (ii) Convert the binary number 1101101.111 into octal number. (iii) Find the 2's complement of the binary number 1011101.10	**03**
	(b)	Explain AND, OR and NOT gates with its truth table, logical expression and logical symbol.	**04**
	(c)	Justify why NAND & NOR gates are known as Universal Logic gates. Design AND, OR & NOT gate using universal logic gates.	**07**
Q.2	**(a)**	Simplify the logical expression: (AB)'(A' + B)(B' + B)	**03**
	(b)	State & prove the De Morgan's theorems using truth table & necessary diagrams.	**04**
	(c)	Define & Explain Binary codes in details with its classification.	**07**
		OR	
	(c)	Explain the CMOS & TTL realization of OR and NOT gates.	**07**
Q.3	**(a)**	Define the terms SOP and POS with examples.	**03**
	(b)	Find the Minterms and Maxterms of the expression Y(A,B,C)= ABC'+ A'B+ AB'C'+ABC	**04**
	(c)	Reduce the expression f(A,B,C,D)=$\sum m$(0,2,5,7,8,10,13,15) using k-map and implement the minimal expression using AND, OR and NOT gates.	**07**
		OR	
Q.3	**(a)**	Define the terms (i) Minterms (ii) Maxterms	**03**
	(b)	Convert the logical expression F(X,Y,Z)=$\sum$m(1,2,3,6) into canonical SOP form.	**04**
	(c)	Reduce the expression f(W,X,Y,Z)=πM(3,5,7,8,10,11,12,13)using k-map and implement the minimal expression using AND, OR and NOT gates.	**07**
Q.4	**(a)**	Draw 1-bit magnitude comparator circuit with its truth table and logical expressions.	**03**
	(b)	Write a short note on PROM.	**04**
	(c)	Explain Full-Adder Circuit in details with truth table, logical expressions and circuit diagram.	**07**
		OR	
Q.4	**(a)**	Draw the logic diagram of 2-4 line decoder circuit.	**03**
	(b)	Design full subtractor using PLA circuit.	**04**
	(c)	Explain Multiplexer (MUX) circuit in details and make design of 8*1 MUX using 4*1 MUX.	**07**

Q.5	**(a)**	Write the difference between Combinational logic circuit and Sequential logic circuit.	**03**
	(b)	Write a short note on Serial-In, Parallel-Out (SIPO) shift register.	**04**
	(c)	Design and explain Asynchronous 2-bit ripple Up and Down counter using Negative Edge-triggered JK Flip-flops.	**07**

OR

Q.5	**(a)**	Draw and explain the working of S-R Latch using NAND gate with truth table.	**03**
	(b)	Write a short note on Master slave flip flop.	**04**
	(c)	Design and explain Synchronous 4-bit Ring counter in details with necessary diagrams.	**07**

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