Seat No.: ________ Enrolment No.___________

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2021

Subject Code:3131102 **Date:21-02-2022**

Subject Name:Digital System Design

Time:10:30 AM TO 01:00 PM **Total Marks:70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Draw the logic circuit for the following Boolean function using NAND gates only. $F(x, y, z) = xy + yz + xz$	**03**
	(b)	State the De-Morgan's Law and find the complement of the following Boolean function in Product-of-Sum (POS) form using De-Morgan's Law. $F(A, B, C, D) = AB'(C+D) + C'D(A'+B)$	**04**
	(c)	Simplify the following Boolean function using **Karnaugh Map (K-map)** method. $F(A, B, C, D) = (A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$ Realize the simplified function using **NOR Gates** only.	**07**
Q.2	**(a)**	State the duality theorem. Also find the dual of the following Boolean expression. $(x + y)(x' + z)(y + z) = (x + y)(x' + z)$	**03**
	(b)	Simplify the following Boolean expression using Boolean Algebra. (i) $x' + xy + xz' + xy'z'$ (ii) $A'B(D' + C'D) + B(A + A'CD)$	**04**
	(c)	Explain the working of Master-Slave SR Flip-flop with Logic diagram and waveforms.	**07**
		OR	
	(c)	Draw the logic circuit of **4-to-1 Multiplexer** and explain its working with the help of truth-table.	**07**
Q.3	**(a)**	Draw truth-table and logic circuit for **2-bit magnitude comparator**.	**03**
	(b)	Explain the following parameters for Digital Integrated Circuits. (i) Fan-out (ii) Fan-in (iii)Propagation Delay (iv)Noise Margin	**04**
	(c)	Find the prime implicants for the following Boolean function by means of the Tabulation Method. $F(A, B, C, D, E) = \Sigma m\ (2, 3, 8, 9, 12, 13, 18, 19, 25, 27, 29, 31)$	**07**
		OR	
Q.3	**(a)**	Explain working of **4-bit Binary Adder circuit** with the neat logic diagram.	**03**
	(b)	Compare TTL and CMOS logic families.	**04**
	(c)	Simplify the following Boolean function **F** together with the don't-care conditions **d** in sum-of-products (SOP) using **Karnaugh Map (K-map)** method. $F(A, B, C, D) = \Sigma m(3, 4, 13, 15)$ and $d(A, B, C, D) = \Sigma m(l, 2, 5, 6, 8, 10, 12, 14)$	**07**

Q.4	**(a)**	State the difference between asynchronous and synchronous sequential logic circuits with suitable example.	**03**
	(b)	What is State Machine? Explain the need of State Machine in Digital Systems.	**04**
	(c)	A sequential circuit with two D flip-flops (***A and B***); one input (***x***); and one output (***y***) is specified by the following state table:	**07**

Present State (AB)	***Next State (AB)***		***Output (y)***	
	x = 0	***x = 1***	***x = 0***	***x = 1***
00	01	00	1	0
01	01	11	0	1
10	00	10	0	1
11	11	10	1	0

Derive the next-state equations, output equation and draw the state diagram.

OR

Q.4	**(a)**	State and explain different types of triggering for Flip-flops.	**03**
	(b)	State the different types of Shift-Registers and explain working of the Serial-In Serial-Out shift register with neat diagram.	**04**
	(c)	Design modulo-10 ripple up counter and explain its working using neat logic diagram and waveforms.	**07**
Q.5	**(a)**	Define: Register, Ripple counter, Synchronous counter.	**03**
	(b)	State various types of **Digital-to-Analog converters** and briefly explain working principle of any.	**04**
	(c)	Draw and explain PLA block diagram. Also draw the Programmable Logic Array with three inputs, three product terms, and two outputs.	**07**

OR

Q.5	**(a)**	Briefly explain the steps for VLSI design flow.	**03**
	(b)	Realize T Flip-flop functionality using D Flip-flop only.	**04**
	(c)	Explain dual slope type **Analog-to-Digital converter** in detail with neat diagram.	**07**

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