Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2020

Subject Code:3130306 Date:05/03/2021

Subject Name:Fundamentals of Digital Electronics

Time:10:30 AM TO 12:30 PM Total Marks:56

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			Marks
Q.1	**(a)**	Define the following terms: (1) Flip flop (2) Counter (3) Register	**03**
	(b)	Implement T flip flop using D flip flop.	**04**
	(c)	Perform the subtraction with the following decimal numbers using 1's compliment and 2's compliments. (a) 11010-1101, (b) 10010-10011	**07**
Q.2	**(a)**	How does a counter work as frequency divider? Explain with suitable example	**03**
	(b)	Draw and explain Ring counter	**04**
	(c)	Write short note on Programmable Logic Arrays.	**07**
Q.3	**(a)**	Reduce the expression F = ((AB)'+A'+AB)'	**03**
	(b)	Convert F (A, B, C) = BC +A into standard minterm form.	**04**
	(c)	Minimise the logic function F (A,B,C,D) = Π_ M (1, 2, 3, 8, 9, 10, 11,14) · d (7, 15) Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only.	**07**
Q.4	**(a)**	Convert the following to other canonical form F(x,y,z) = Σ(1,3,7)	**03**
	(b)	Discuss NAND gate as universal gate (implement NOT, AND, OR & NOR gate using NAND gate)	**04**
	(c)	State and prove De'Morgan's Theorems with the help of truth tables.	**07**
Q.5	**(a)**	Give the applications of Decoder.	**03**
	(b)	Implement the given function using multiplexer F(A,B,C) = Σm(1,2,4,7)	**04**
	(c)	Implement following logic function using 8X1 MUX. F = Σ m(0, 1, 3, 5, 7, 11, 13, 14, 15)	**07**
Q.6	**(a)**	Explain the working of multiplexer	**03**
	(b)	Design 4 X 16 decoder using two 3 X 8 decoder.	**04**
	(c)	Design a 8 to 1 multiplexer by using the four variable function given by F(A,B,C,D) =Σm(0,1,3,4,8,9,15).	**07**
Q.7	**(a)**	Explain Johnson counter.	**03**
	(b)	Draw & explain in brief a high assertion input SR latch.	**04**
	(c)	With logic circuit explain the working of 4-bit magnitude comparator.	**07**
Q.8	**(a)**	Explain shift registers.	**03**
	(b)	What is race around condition in JK flip flop.	**04**
	(c)	Explain half and full adders in detail.	**07**

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