Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2020

Subject Code:3131102 Date:04/03/2021

Subject Name:Digital System Design

Time:10:30 AM TO 12:30 PM Total Marks:56

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	State and prove De-Morgan's Theorem.	**03**
	(b)	Explain Moore machine.	**04**
	(c)	Simplify the following Boolean expression by means of the Tabulation method. $F(A,B,C,D) = \sum m\ (1,2,3,5,6,7,8,9,12,13,15)$.	**07**
Q.2	**(a)**	Give comparison of TTL and CMOS family.	**03**
	(b)	Implement the given function using 8 X 1 multiplexer. $F(A,B,C,D) = \sum m\ (0,1,2,3,5,8,9,11,14)$.	**04**
	(c)	Design synchronous BCD counter using JK flip flop.	**07**
Q.3	**(a)**	Explain universal gates.	**03**
	(b)	Compare ROM, PLA and PAL.	**04**
	(c)	Design a counter to generate the repetitive sequence 0,1,2,4,3,6.	**07**
Q.4	**(a)**	Explain half adder circuit.	**03**
	(b)	Convert SR Flip Flop to JK Flip Flop.	**04**
	(c)	Design a counter to generate the repetitive sequence 0,3,5,7,4.	**07**
Q.5	**(a)**	Define: i) Fan-in ii) Fan-out iii) Propagation delay	**03**
	(b)	Construct a Johnson counter with ten timing signals.	**04**
	(c)	Design BCD to Excess 3 code converter.	**07**
Q.6	**(a)**	Compare combinational and sequential logic circuits.	**03**
	(b)	Explain different modeling styles in Verilog.	**04**
	(c)	Explain Dual Slope A/D converter in detail.	**07**
Q.7	**(a)**	Describe magnitude comparator.	**03**
	(b)	Express the Boolean function F=AB+A'C in a product of max term.	**04**
	(c)	Explain Emitter Coupled Logic (ECL) in detail.	**07**
Q.8	**(a)**	Explain briefly 3 line to 8 line decoder.	**03**
	(b)	Explain Mealy machine.	**04**
	(c)	Write a short note on 4-bit Universal Shift Register.	**07**

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