GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER– III (New) EXAMINATION – WINTER 2019

Subject Code: 3130306   **Date: 3/12/2019**
Subject Name: Fundamentals of Digital Electronics
Time: 02:30 PM TO 05:00 PM   **Total Marks: 70**
Instructions:
   1. **Attempt all questions.**
   2. **Make suitable assumptions wherever necessary.**
   3. **Figures to the right indicate full marks.**

			Marks
Q.1	**(a)**	Subtract the following binary numbers by the 2's and 1's complement method. 10110-1011	**03**
	(b)	Encode data bits 1011 into the 7-bit even parity Hamming code. Find and correct error from 7-bit hamming code given below. 1110110	**04**
	(c)	Explain TTL and CMOS realization of AND and OR gate.	**07**
Q.2	**(a)**	For a two input AND & OR gate, Determine its output waveform in relations to input waveform A & B. Input A has frequency 2Hz with duty cycle 50% and Input B has frequency 1Hz with duty cycle 70%.	**03**
	(b)	Explain EX-OR and EX-NOR gate using its truth table, Symbol, and logic diagram.	**04**
	(c)	Reduce the expression f=$\sum m(1,4,7,10,13) + d(5,14,15)$ using k-map and implement the minimal expression in universal logic.	**07**

OR

	(c)	Find the minimal expression for $f = \prod M(2,8,9,10,11,12,14)$ using tabular method.	**07**
Q.3	**(a)**	Reduce the Boolean Expression: $f = AB + \overline{AC} + A\bar{B}C(AB + C)$.	**03**
	(b)	Design 4-input priority encoder.	**04**
	(c)	Design Half adder and Half subtractor using universal logic.	**07**

OR

Q.3	**(a)**	Draw logic diagram of 3-8 line decoder.	**03**
	(b)	Find out Minterms and Maxterms for Boolean expression: $f = A(\bar{A} + \bar{B})(A + B + C)$.	**04**
	(c)	Implement the logic function F=$\sum m(0,1,2,3,4,10,11,14,15)$ using a 16:1 MUX and 8:1 MUX.	**07**
Q.4	**(a)**	Explain 1-bit Magnitude comparator with logic diagram.	**03**
	(b)	Design full adder using PAL circuit.	**04**
	(c)	Design a 4-bit Binary to Gray Code converter with logic diagram.	**07**

OR

Q.4	**(a)**	Write comparison of programmable logic devices.	**03**
	(b)	Design full subtractor using PLA circuit.	**04**
	(c)	Explain design of a synchronous 3-bit Up-Down counter using J-K flip-flops.	**07**
Q.5	**(a)**	Write comparison between synchronous and asynchronous sequential circuits.	**03**
	(b)	Describe master-slave pulse triggered D-flip-flop.	**04**
	(c)	Explain edge-triggered J-K flip-flop and T-flip-flop.	**07**

OR

Q.5	**(a)**	Write excitation tables of S-R, J-K, D, and T flip-flop.	**03**
	(b)	Describe Serial In, Parallel Out shift register.	**04**
	(c)	Design and explain Asynchronous two bit ripple up and down counter using negative edge triggered J-K flip-flops.	**07**

****