Seat No.:	Enrolment No.

## **GUJARAT TECHNOLOGICAL UNIVERSITY**

**BE - SEMESTER-III(NEW) EXAMINATION - SUMMER 2023** 

	•	Code:3130306 Date:01-08-20	)23
		Name: Fundamentals of Digital Electronics	
		2:30 PM TO 05:00 PM Total Marks	s:70
Ins	tructio 1	ons: Attempt all questions.	
		Make suitable assumptions wherever necessary.	
	3.	Figures to the right indicate full marks.	
	4.	Simple and non-programmable scientific calculators are allowed.	MARKS
Q.1	(a)	Subtract the following decimal numbers using 2's complement method, 52-17.	03
	<b>(b)</b>	Explain EX-OR and EX-NOR gate.	04
	(c)	Explain AND, OR, NOT, NAND and NOR gate with truth table, symbol. Why	07
		NAND & NOR gates called Universal gates?	
Q.2	(a)	Encode data bits 1101 into the 7-bit even parity Hamming code.	03
	<b>(b)</b>	Reduce the expression $f = A + B[AC + (B + \bar{C})D]$	04
	<b>(c)</b>	Explain Classification of Binary codes.	07
	(a)	OR  Explain Evil adden in detail	07
	(c)	Explain Full adder in detail.	U/
Q.3	(a)	Draw logic diagram of Boolean expression $f = A + A\overline{B} + \overline{ABC} + B\overline{C}$ .	03
	<b>(b)</b>	Expand $f = A (A+B+C)$ to maxterms and minterms.	04
	(c)	Use a Multiplexer to implement the logic function $= A \oplus B \oplus C$ . <b>OR</b>	07
<b>Q.3</b>	(a)	Explain SOP and POS representation of Boolean Expression.	03
	(b)	Write Comparison of PLA, PAL and PROM.	04
	(c)	Find the minimal expression for $f = \sum m\{2,3,8,12,13\} + d(10,14)$ using Kmap.	07
		Kinap.	
<b>Q.4</b>		Define Fan in, Fan out, Propagation Delay.	03
		Describe Octal to Binary Encoder.	04
	<b>(c)</b>	Design 4-bit Binary to Gray Code Converter.  OR	07
Q.4	(a)	Explain T Flip –flop.	03
<b>~</b> ··	<b>(b)</b>	Describe Master- Slave S-R flip flop.	04
	<b>(c)</b>	Using the tabular method, obtain the minimal expression for $f =$	07
		$\sum m\{6,7,8,9\} + d(10,11,12,13,14,15).$	
Q.5	(a)	Subtract the following decimal numbers using 9's complement method,	03
		524.7-17.5	
	<b>(b)</b>	Explain Ring counter.	04
	(c)	Explain negative edge triggered JK flip-flop.  OR	07
Q.5	(a)	Prove De morgan theorem by using Truth table.	03
· ·	<b>(b)</b>	Explain Serial IN, Serial Out shift register.	04
	<b>(c)</b>	Design Synchronous 3-bit Down Counter using JK flip flop.	07

\*\*\*\*\*