GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III (NEW) EXAMINATION - SUMMER 2021			
Subject Code:3130306 Date:14/09/			/2021
Subject Name: Fundamentals of Digital Electronics			
Time:10:30 AM TO 01:00 PM Total Marks:'			ks:70
Instructions:			
	1. 2. 3. 4.	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks. Simple and non-programmable scientific calculators are allowed.	
			Marks
Q.1	(a)	Define the following terms: (1) Buffer Register (2) Flip flop (3) Counter	03
	(b)	Explain S-R Latch.	04
	(c)	Perform the subtraction with the following decimal numbers (a) 14 from 25 using 8bit 1's compliment (b) 14 from 46 using 8 bit 2's compliments.	07
Q.2	(a)	How does a counter work as frequency divider? Explain with suitable example	03
	(b)	Explain Johnson counter.	04
	(c)	Compare ROM, PLA and PAL.	07
	(c)	UR Write short note on Programmable Logic Arrays	07
03	(\mathbf{c})	Show that $AB+AB'C+BC' = AC+BC'$	07
Q.3	(a) (b)	Discuss NAND gate as universal gate (implement NOT AND OR &	03
	()	NOR gate using NAND gate)	07
	(C)	Keduce using mapping the Expression $\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and implement it in universal logic	07
		OR	
Q.3	(a)	Convert the following to other canonical form	03
		$F(x,y,z) = \Sigma(1,3,7)$	
	(b)	Convert the following expression into sum of products and products of sums: (BC + D)(C + AD')	04
~ ((c)	State and prove De'Morgan's Theorems with the help of truth tables.	07
Q.4	(a)	Give the applications of Decoder. Implement the given function using multipleyer $E(w, y, y, z) = \Pi(2, 10)$	03
	(U)	11) Indication using multiplexer $F(w, x, y, z) = \prod(5, 10, 11)$	04
	(c)	Implement following logic function using 8X1 MUX. $P = \Sigma m(1, 2, 6, 7, 8, 10, 13, 14)$	07
OR OR			
Q.4	(a) (b)	Explain the working of multiplexer	03
	(U) (C)	Design 4 X to decoder using two 5 X 8 decoder.	04
	(C)	$F(A,B,C,D) = \Sigma m(0,1,3,4,8,9,15).$	07
Q.5	(a)	Draw and explain Ring counter in brief.	03
-	(b)	What is race around condition in JK flip flop.	04
	(c)	With logic circuit explain the working of 4-bit magnitude comparator. OR	07
Q.5	(a)	Explain shift registers.	03
	(b)	Draw & explain in brief a high assertion input SR latch.	04
	(c)	Explain half and full adders in detail.	07
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