

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE - SEMESTER-III (NEW) EXAMINATION – SUMMER 2021****Subject Code:3130907****Date:11/09/2021****Subject Name:Analog & Digital Electronics****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

		MARKS
<b>Q.1</b>	(a) Draw transistor C-E amplifier circuit. Draw its ac equivalent circuit.	<b>03</b>
	(b) Sketch the block schematic of a typical operational amplifier and briefly explain the function of each block.	<b>04</b>
	(c) Explain how Op-amp works as summing amplifier.	<b>07</b>
<b>Q.2</b>	(a) List applications of instrumentation amplifier.	<b>03</b>
	(b) Explain the following terms. (1) PSRR (2) Input bias current (3) Input offset Voltage (4) CMRR.	<b>04</b>
	(c) Explain in detail voltage follower with its applications.	<b>07</b>
<b>OR</b>		
<b>Q.3</b>	(a) What are the advantages of active filters over passive filters?	<b>03</b>
	(b) Sketch Wein bridge oscillator. Explain working.	<b>04</b>
	(c) Draw the circuit op-amp as differentiator and explain with necessary waveforms.	<b>07</b>
<b>OR</b>		
<b>Q.3</b>	(a) How to detect peak of waveform using OP-AMP?	<b>03</b>
	(b) Compare: Comparator and Schmitt trigger.	<b>04</b>
	(c) Draw and explain the use of op-amp as a zero crossing detector.	<b>07</b>
<b>Q.4</b>	(a) Compare SOP and POS.	<b>03</b>
	(b) Write short note on Gray code.	<b>04</b>
	(c) Prove that NAND and NOR gates are universal gates.	<b>07</b>
<b>OR</b>		
<b>Q.4</b>	(a) Design half subtractor logic circuit.	<b>03</b>
	(b) Explain Master-Slave J-K flip-flop configuration.	<b>04</b>
	(c) Simplify the Boolean function $F(A,B,C,D) = \sum m (2,5,7,8,11,14,15)$ , $\sum d=(0,3,6,10)$ using K-map method. Implement using basic logic gates.	<b>07</b>
<b>Q.5</b>	(a) Sketch sample and hold circuit and explain its working.	<b>03</b>
	(b) Explain resolution and quantization error in reference to ADC.	<b>04</b>
	(c) Design 4-bit up/down ripple counter.	<b>07</b>
<b>OR</b>		
<b>Q.5</b>	(a) Compare EPROM with FLASH memory.	<b>03</b>
	(b) Explain R-2R ladder DAC with necessary diagram.	<b>04</b>
	(c) Draw 4-bit down counter; explain its working with timing diagram and truth table.	<b>07</b>

\*\*\*\*\*